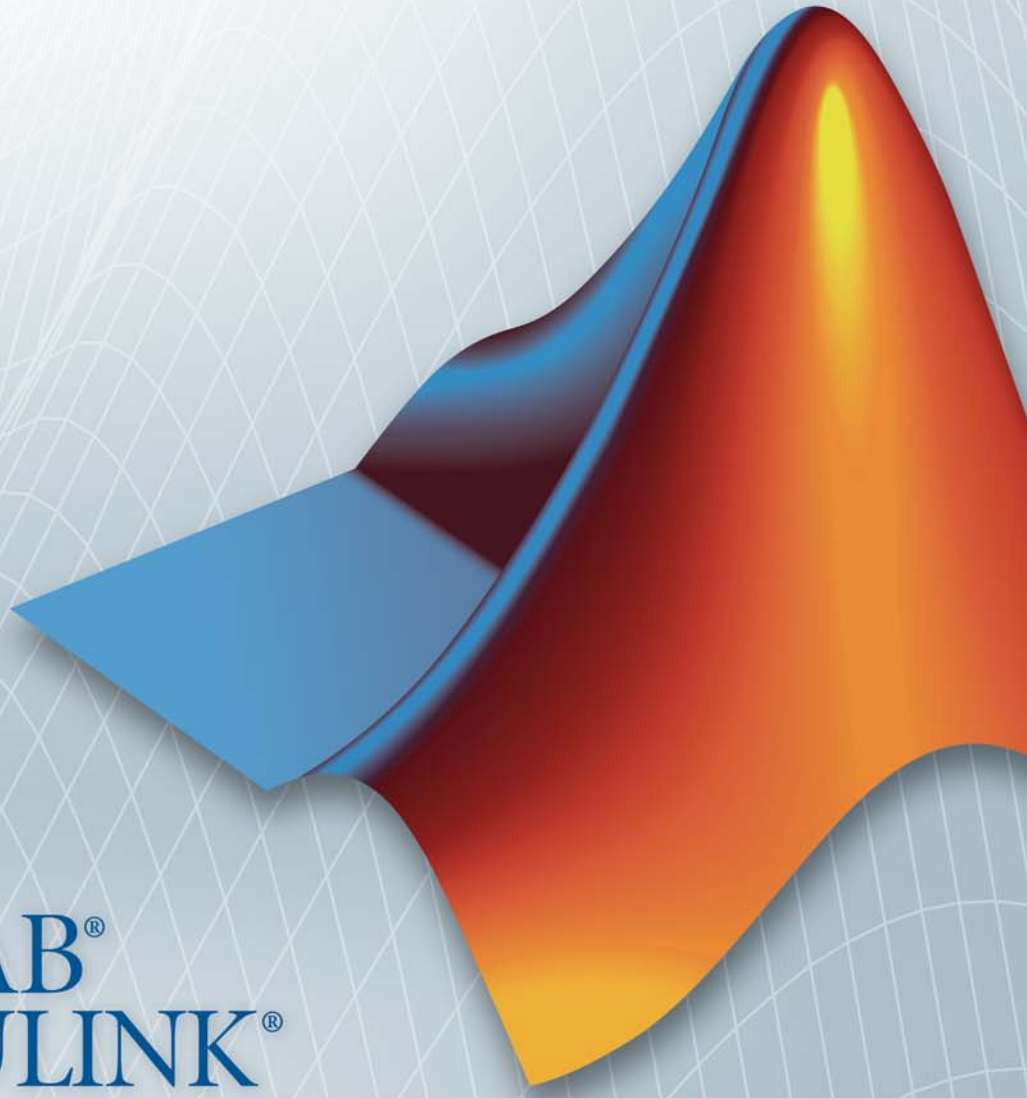
HDL Verifier™

Getting Started Guide

R2012b



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HDL Verifier™ Getting Started Guide

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Introduction

Product Description

Verify VHDL® and Verilog® using HDL simulators and FPGA-in-the-loop test benches

HDL Verifier™ automates Verilog and VHDL design verification using HDL simulators and FPGA hardware-in-the-loop. It provides interfaces that link MATLAB® and Simulink® with Cadence Incisive®, Mentor Graphics® ModelSim®, and Mentor Graphics Questa® HDL simulators. It also supports FPGA-in-the-loop verification with Xilinx® and Altera® FPGA boards.

HDL Verifier automates verification by using MATLAB or Simulink to stimulate your HDL code and analyze its response. This approach eliminates the need to author standalone Verilog or VHDL test benches.

Key Features

- Cosimulation support for Cadence Incisive and for Mentor Graphics ModelSim and Questa
- FPGA-in-the-loop verification using Xilinx and Altera FPGA boards
- MATLAB functions and Simulink blocks
- Generation of IEEE® 1666 SystemC TLM 2.0 compatible transaction-level models
- Interactive or batch-mode cosimulation and debugging
- Single-machine, multiple-machine, and cross-network cosimulation

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Third-Party Product Requirements

Supported EDA Tools

In this section...

"Cosimulation Requirements" on page 2-2

"FPGA Verification Requirements" on page 2-3

Cosimulation Requirements

- "Cadence Incisive Requirements" on page 2-2
- "Mentor Graphics Questa and ModelSim Usage Requirements" on page 2-2

Cadence Incisive Requirements

MATLAB and Simulink support Cadence® verification tools using HDL Verifier. Use one of these recommended versions, which have been fully tested against the current release:

- ES 10.2-s040
- IES 9.2-s014
- IUS 8.2-s009
- IUS 11.10-s005

The HDL Verifier shared libraries (`liblfihdls*.so`, `liblfihdlc*.so`) are built using the gcc included in the Cadence Incisive simulator platform distribution. Before you link your own applications into the HDL simulator, first try building against this gcc. See the HDL simulator documentation for more details about how to build and link your own applications.

Mentor Graphics Questa and ModelSim Usage Requirements

MATLAB and Simulink support Mentor Graphics verification tools using HDL Verifier. Use one of the following recommended versions. Each version has been fully tested against the current release:

- ModelSim SE 10.0c, 6.6d, 6.5f

- ModelSim PE 10.0c, 6.6d, 6.5f
- ModelSim DE 10.0c
- Questa 10.0a

TheLinux® platform requires that HDL Verifier software run gcc c++ libraries (4.1 or later). You should install a recent version of the gcc c++ library on your computer. To determine which libraries are installed on your computer, type the command:

```
gcc -v
```

FPGA Verification Requirements

- "Xilinx ISE Usage Requirements" on page 2-3
- "Altera Quartus II Usage Requirements" on page 2-3
- "Supported FPGA Devices for FIL Simulation" on page 2-4
- "Supported FPGA Device Families for Clock Module Generation" on page 2-4

Xilinx ISE Usage Requirements

MATLAB and Simulink support Xilinx design tools using HDL Verifier.

- FPGA-in-the-Loop and FPGA Automation are tested with Xilinx ISE 13.4.
- ISE 11.1 or newer is recommended
- Additional requirements for clock module generation using FPGA Automation:
  - 12.1 or later: Windows® only
  - 11.4: Windows 32-bit only
- Consult Xilinx user documentation for compatibility of ISE tools with various Linux distributions.

Altera Quartus II Usage Requirements

MATLAB and Simulink support Altera design tools using HDL Verifier.

- FPGA-in-the-Loop is tested with Altera Quartus II 11.0.

Supported FPGA Devices for FIL Simulation

HDL Verifier supports FIL simulation on the devices shown in the following table.

Device Family	Board
Spartan-6	Spartan-6 SP605 Spartan-6 SP601 XUP Atlys Spartan-6
Virtex-6	Virtex-6 ML605
Virtex-5	Virtex-5 ML505 Virtex-5 ML506 Virtex-5 ML507 Virtex-5 XUPV5–LX110T
Virtex-4	Virtex-4 ML401 Virtex-4 ML402 Virtex-4 ML403
Altera	Arria II GX FPGA development kit Cyclone III FPGA development kit Cyclone IV GX FPGA development kit DE2-115 development and education board

Supported FPGA Device Families for Clock Module Generation

For project generation with Filter Design HDL Coder™, see Xilinx documentation for a full list of supported FPGA families in ISE.

With the current release, clock module generation is supported for the following device families:

- Spartan-3
- Spartan-3A and Spartan-3AN

- Spartan-3A DSP
- Spartan-3E
- Spartan-6
- Virtex-4
- Virtex-5

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